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A 12. Moore's Law and the Design of Computer Chip's

A Materials Perspective

by Conall Daly

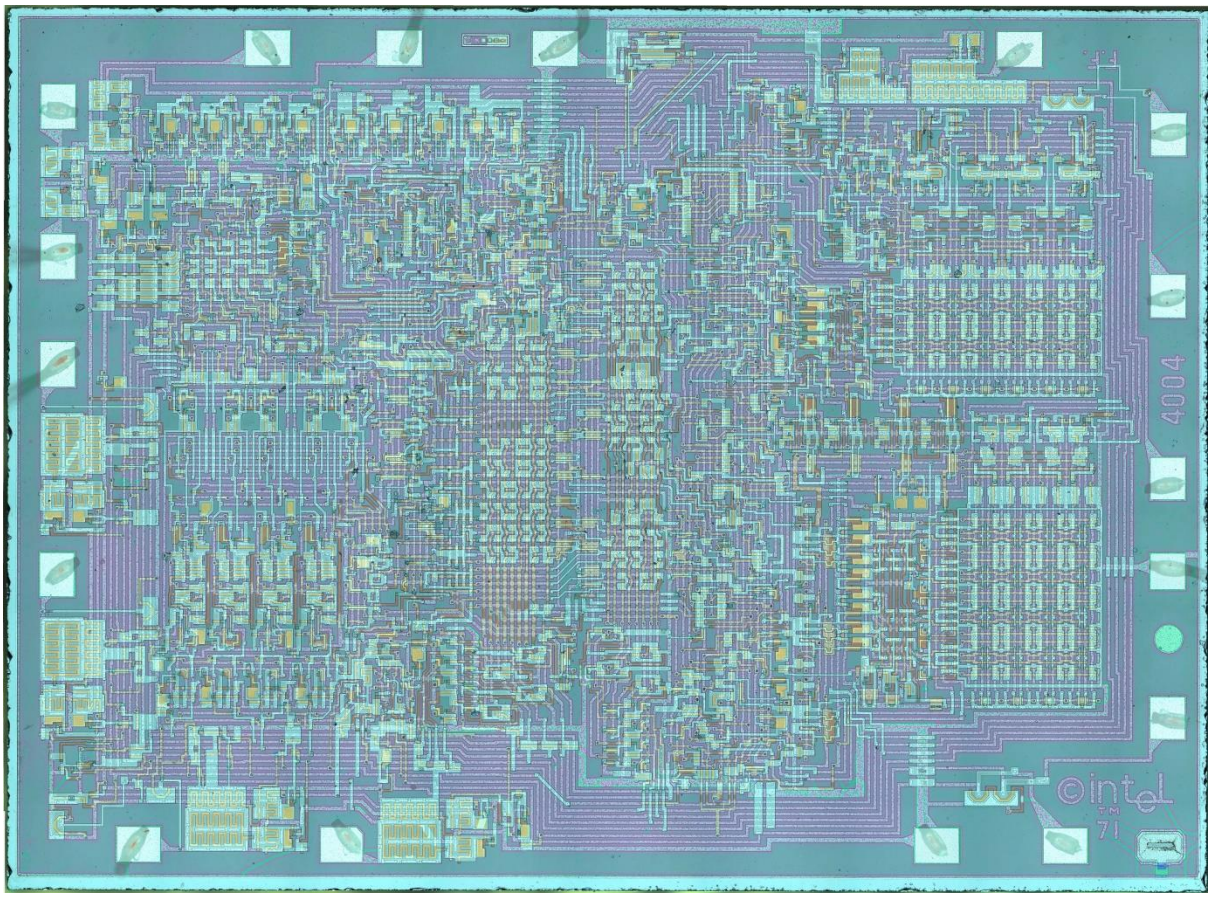


Fig. 1. Die Shot of the first commercially produced microprocessor, the Intel 4004

1. Summary

"Because of the nature of Moore's law, anything that an extremely clever graphics programmer can do at one point can be replicated by a merely competent programmer some number of years later" **[Web. 1.]**

-John Carmack, Founder of id Software and CTO of Oculus VR

The quote above really encapsulates the importance of Moore's Law to the performance of modern-day software and up until quite recently it accurately predicted advances in computer chips. With the advent of computationally intensive tasks such as finite element analysis and computational fluid dynamics in the engineering world and deep neural networks in computer science, the end of Moore's law essentially means an end to human progress.

This report will examine the current design techniques used for computer chips to get the most out of MOS (Metal Oxide Semiconductor) based gates and look at the key material properties for a semiconductor along with looking at how exactly the transistor may be reaching its limits. We will also examine current and future manufacturing methods of computer chips detailing the Czochralski technique for semiconducting crystal formation and lithographic technology for feature patterning.

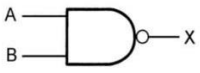
We'll examine the ways in which failure can occur within electronic devices and the many ways in which we can predict failure through analysis and most pertinent to us how device scaling effects failure. We'll also address the pressing issue of recyclability of electronic devices and see exactly how the myriad of materials that go into electronic devices can be recovered and whether there is more that could be done.

Finally, we will examine the "end of life" of silicon chips as we know them and look at what new techniques could side-step Moore's Law altogether and examine the material advances required for the implementation of quantum computation chips.

2. Materials Design Aspects of Computer Chips

To begin we'll examine what properties it is we must have in mind when designing the devices that go into realising a computer chip. We'll examine the desired electronic properties of materials how we can modify the material parameters of semiconductors to get them in a state for manufacturing.

2.1. The Transistor Device



A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2. NAND Gate Logic Block Representation

Almost all modern digital computing is performed via the logic gate depicted in **Fig. 2.** above which allows, through combination of multiple NANDs, the construction of any logic operation we want. However, we are interested in the physical and material considerations of this device and so must look deeper to see the material principles that allow this device to operate.

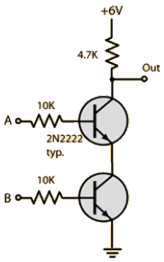


Fig. 3. Transistor Representation of a NAND Gate

To perform logic operations, we implement an idea very similar to a lightbulb and switches [Lit. 1.]. Imagining the bulb as the NAND gate output and the two relays acting as the transistor inputs we can see we need a "fast switch" so to speak that gives us the ability to read data at high speeds and allows gates to act upon other gates, chaining them

together to create arithmetic logic units and random access memory and hence build up to a central processing unit or "computer chip". What material could provide such a function?

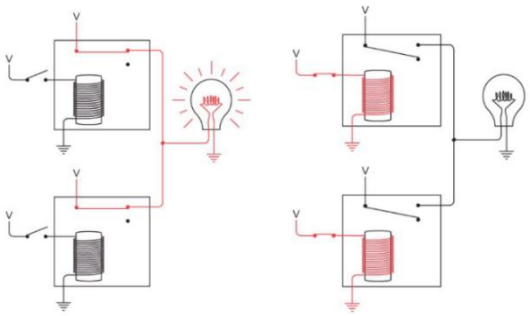


Fig. 4. Lightbulb Representation of a NAND Gate

2.2. Electronic Materials and their Properties

For solid-state electrical devices such as the transistor we are primarily interested in the electrical properties of solid materials, specifically we are interested in how charge is transported through semiconductors which is dependent on both the properties of the electron and the arrangement of atoms within its crystal lattice.

2.2.1. Structure of Semiconductors

Semiconductors possess the property of having conductance's in between those of insulators and metals, this is one interesting property that makes them suitable for our purposes of creating transistors where we would like to control the flow of electrons i.e. allowing us to switch the flow on and off.

Fig. 5. Common Semiconductor Materials

Elemental	IV Compounds	Binary III-V Compounds	Binary II-VI Compounds
Si	SiC	AlP	ZnS
Ge	SiGe	AlAs	ZnSe
		AlSb	ZnTe
		GaN	CdS
		GaP	CdSe
		GaAs	CdTe
		GaSb	
		InP	
		InAs	
		InSb	

The most common semiconductors are the elemental semiconductors, which are composed of a single species of atoms, these are Silicon and Germanium, located in column IV of the periodic table. Germanium was quite a popular semiconductor material but has since been replaced by Silicon for most semiconductor applications.

Other semiconductors are primarily obtained through creating compound elements such as Gallium Arsenide, these semiconductors "are widely used in high-speed applications and devices requiring the emission or absorption of light" [Lit. 2.]

The elemental semiconductors are derived from the *diamond* lattice structure and the compounds semiconductors derive from the altered diamond lattice (zincblende) structure which is made up of two elements. It is also worth noting that some of the II-VI compound semiconductors derive from a wurtzite lattice.

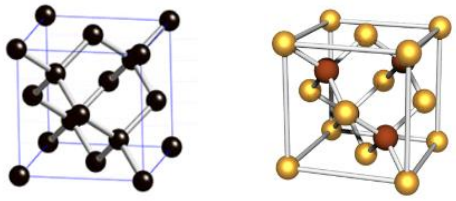


Fig. 6. Diamond Lattice (Left) and Zincblende Lattice (Right)

Some crystal structure considerations also apply to the processing of Silicon crystals such as the orientation of the crystal. Oxidation is an important process during semiconductor manufacturing, which allows layers of conductors and insulators to be layered on top of the substrate before pattern transfer and etching. As such {111} planes oxidize faster than {100} planes because the former has a higher number of atoms per unit of surface area available for the oxidation reaction to act on [Lit. 3.].

Another consideration for those designing the material properties of chips is how defects affect the manufacturing of the semiconductor wafer. Like metals semiconductors can have point defects which can affect the properties of the material.

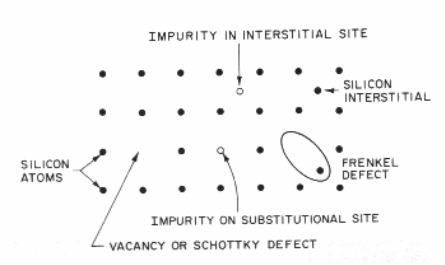


Fig. 7. Point Defects in a Silicon Lattice

Vacancies and interstitials have equilibrium concentrations that depend on temperature which can be calculated via the following equation derived from thermodynamic principles:

$$N_d = A\,exp\left(-\frac{E_a}{kT}\right)$$

Eq. 1. Defect Concentration

where:

$$N_d = Concentration\ of\ the\ Point\ Defect$$
$$A = Concentration\ of\ Atomic\ Sites$$
$$E_a = Activation\ Energy\ of\ the\ Point\ Defect$$
$$k = Boltzmann\ Constant$$
$$T = Absolute\ Temperature\ in\ Kelvin$$

The diffusion of impurities and the oxidation rate of silicon depend greatly on the concentrations of these defects. Next, we will look at how these defects re utilized to carry electrical charge within a semiconductor and how current flows within them.

2.2.2. Energy Bands and Charge Carriers

Since Einstein's work on the photoelectric effect which won him a Nobel Prize in 1921, we have known that electrons occupy discrete energy levels in their electronic structures. However, for solids where atoms aren't isolated electrons have a band of available energies it can occupy. This is caused by interactions between the wave functions of the electrons within the material, where the wavefunction refers to the probability function given by solving the Schrödinger

Equation and finding $\boldsymbol{\Psi}$ for the boundary conditions of an electron giving us the probability of finding that specific electron at a certain position in space.

$$-\frac{h}{4\pi m}\boldsymbol{\nabla^2\Psi} + \boldsymbol{V\Psi} = -\frac{h}{2\pi i}\frac{\partial \boldsymbol{\Psi}}{\partial t}$$

Eq. 2. The 3-D Schrodinger Wave Equation

where:

$$h = Plancks\ Constant$$

$$m = Mass\ of\ the\ Electron$$

$$\nabla^2\boldsymbol{\Psi} = \frac{\partial^2\boldsymbol{\Psi}}{\partial x^2} + \frac{\partial^2\boldsymbol{\Psi}}{\partial y^2} + \frac{\partial^2\boldsymbol{\Psi}}{\partial z^2}$$

$$\boldsymbol{\Psi} = Wavefunction\ in\ Vector\ Form$$

$$\boldsymbol{V} = Potential\ Energy\ of\ Electron\ in\ Vector\ Form$$

For individual atoms these electron wave functions and therefore electronic structures can be identical. However, in solids wavefunctions between atoms interact. From the Pauli Exclusion Principle, we know that no two electrons in a system can occupy the same quantum state therefore the discrete energy levels split creating a larger electronic structure with more levels for the two-atom system.

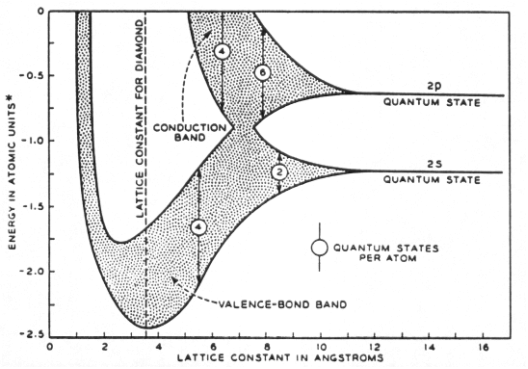


Fig. 8. Energy Levels in Silicon as a Function of Interatomic Spacing

We can imagine that as we add more and more atoms to eventually arrive at a full scale solid that these energy levels overlap so much that they essentially create continuous energy bands that the electrons can occupy. All solids have their own

unique energy band structure and the three main ones we want to examine are shown in **Fig. 9.**

At O° Kelvin, semiconductors have basically the same band structure as an insulator, so current cannot be transported between or in the bands as all the electron states are occupied.

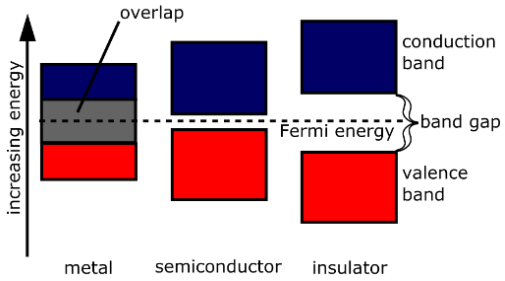


Fig. 9. Energy Bands of Three Electronic Materials

However, a semiconductor has a much smaller bandgap of roughly 1 eV compared to insulators which are on the order of 10 eV and so electrons can be agitated by thermal or optical energy which allows them to "jump" the bandgap allowing the transport of charge. The introduction of impurities plays an important role in determining the structure of a semiconductor's energy band.

Current flow in semiconductors is purely dictated by the movement of charge carriers known as "electrons" and "holes". Holes are a rather abstract concept and is simply the absence of an electron but is treated as a charge carrier in electronic materials analysis.

We must delineate between intrinsic and extrinsic semiconducting materials. Silicon without any impurities or lattice defects is known as intrinsic Silicon and is essentially the "feedstock" that materials designer work with and adjust material properties to obtain extrinsic Silicon. Extrinsic Silicon is semiconducting material that has been "doped", this is mainly what we work with in the manufacturing stage. By introducing impurities and lattice defects into the crystal lattice on purpose, we can adjust the size of the conduction and valence bands thereby controlling the

conductivity of the semiconductor. We can create either a predominance of holes or electrons in the semiconductor which are known respectively as p-type and n-type semiconductor. As an example of how drastically electronic properties can change with doping if we dope Silicon with 10^{15} As atoms/cm^3 the resistivity of Silicon changes from about 2×10^5 Ω-cm to 5 Ω-cm [Lit. 2.]. We'll examine the doping process in more detail in the manufacturing considerations.

2.3. Realising a Transistor with Electronic Materials

Now that we have a material with properties that we can control we will examine the physical device that is to be created, the field-effect transistor (FET). The simplest transistor which we will consider is the junction field-effect transistor (JFET) however in practice the MOSFET (metal oxide semiconductor field-effect transistor) and CMOS (complementary metal oxide semiconductor) are the most widely used technologies in modern semiconductor manufacturing due to their high input impedances, which is ideal for high speed conducting and non-conducting switching in digital circuitry.

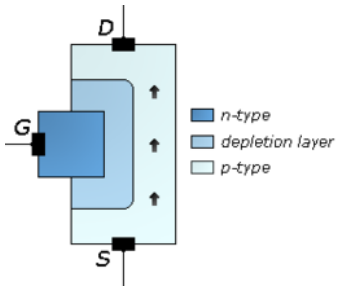


Fig. 10. Junction Field-Effect Transistor

In general, all transistors work on the principle of varying the width of the depletion region, which is a barrier of fully occupied electron-hole states, via an applied voltage at the gate (n-type region in diagram). At first the bipolar junction transistor was the first transistor technology invented by Bardeen, Brattain and Shockley in 1948. However, it was only through the work of Mohammed M. Atalla at Bell Labs in the late 1950's that showed the importance of controlling surface defects in the Silicon through the application of an SiO_2 layer hence the creation of the metal **oxide** field effect transistor [Lit. 4.]. The field effect allowed for greater miniaturization and the unprecedented pace of Moore's Law.

2.4. Moore's Law

Gordon Moore first made his now ubiquitous observation on the rate of progress of the semiconductor field in Electronics Magazine in 1965 and is best illustrated in the graph included by Moore in his article shown in **Fig. 11.** That the number of transistors on a Silicon would double every 18 months**.** It is quite amazing that Moore's Law has held for the past 50 years and was a truly unprecedented rate of progress that had never been seen in any industry previous. However, we have reached a fundamental limit where Moore's Law is beginning to deviate as actual transistor count increase is beginning to slow. Despite the best efforts of Intel and TSMC [Web. 2.] we must confront the reality that we have reached the atomic level and need to radically change semiconductor processes to continue to innovate.

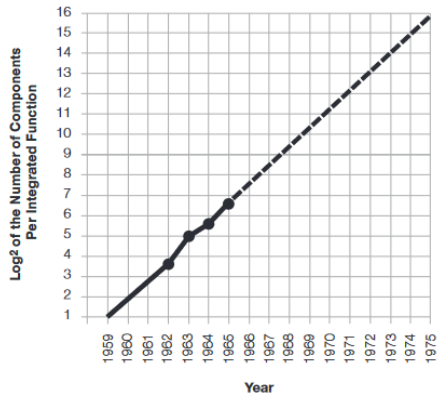


Fig. 11. Log Transistor Count on Integrated Circuit versus Year "Moore's Law"

Moore's Law faces challenges on many fronts in the final part of this materials section we will look at the challenge posed by quantum mechanics. Later we will discuss how lithographic processes are reaching their limits and will consider device scaling aspects in terms of failure modes.

2.5. The Problem Posed by Quantum Mechanics

The primary size the semiconductor industry wants to shrink is the distance between the source and the drain electrodes. Currently this stands at around 5 nanometres fabricated by Samsung and TSMC.

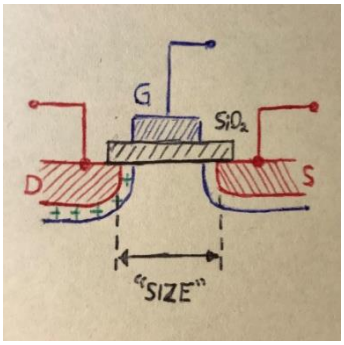


Fig. 12. Transistor "Size"

We know the atomic radius of Silicon is 0.111 nm so doing a quick calculation:

$$\frac{5\ nm}{2\ \times 0.111\ nm} \approx 22\ Silicon\ Atoms$$

Currently 22 Silicon atoms separate the gate from the source. As this size shrinks down to the atomic level it becomes increasingly more difficult to keep electrons from quantum tunnelling between the source and drain [Lit. 6.]. The engineering problem lies in creating a high enough potential barrier to stop this effect.

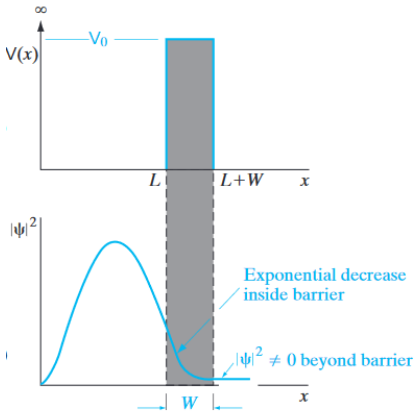


Fig. 13. Electron Wavefunction, Potential Barrier and Quantum Tunneling Effect

Some progress has been made in doing this using molecular electronic devices which employ quantum interference to stop the electrons from tunnelling [Lit. 7.]. However, it is not practical for the purposes of manufacturing yet. We will explore more avenues for circumventing Moore's Law in the last section.

3. Semiconductor Chip Fabrication

Semiconductor fabrication is one of the most complex manufacturing processes that takes place on the planet so in this section we will talk about the main methods of crystal manufacturing and of semiconductor device fabrication but be aware there is far more detail that goes into chip manufacturing.

3.1. Crystal Preparation

The first step in the Silicon chip fabrication process involves growing the crystal substrate onto which conductors and inductors will be layered, transistors will be patterned and later etched.

3.1.1. Czochralski Technique

80 – 90% of Silicon crystals for the semiconductor industry are grown via the Czochralski technique [Lit. 3.]. The growth of crystal basically involves a phase change of a solid, liquid or gas phase to a solid crystalline phase. Growing a Czochralski crystal requires the solidification of atoms in a liquid phase at a crystal growth interface, of course this requires the growth of a "seed crystal" grown via a different method to begin the process.

Fig. 14. Czochralski Crystal Crucible and Puller Device

The two most important process parameters are the pull rate and the growth rate of the crystal. The pull rate is the speed at which the solid crystal is pulled out of the melt and is determined via **Eq. 3.**

$$V_{max} = \frac{k_s}{Ld}\frac{dT}{dx}$$

Eq. 3. Crystal Pull Rate

where:

$$k_s = Thermal\ Conductivity\ of\ Solid\ to\ be\ Crystallised$$

$$L = Latent\ Heat\ of\ Fusion$$

$$d = Density\ of\ Solid\ to\ be\ Crystallised$$

$$\frac{dT}{dx} = Thermal\ Gradient\ in\ the\ Melt$$

In practice the pull rate is about 30% to 50% slower [Lit. 3.] than the theoretical maximum obtained from **Eq. 3.** Pull rate indicates macroscopically the net solidification rate of the crystal whereas growth rate indicates the instantaneous solidification rate. Both parameters influence the generation of impurities in the crystal, such as defect structure and dopant distribution. Crystals are put through a resistivity check using a four-point probe technique to ensure the desired resistivity is achieved.

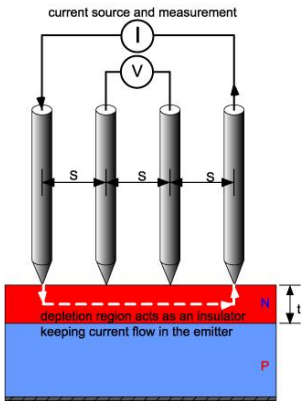


Fig. 15. Four-Point Probe Resistivity Measurement

3.1.2. Doping, Ion Implantation and Carrier Concentrations

To create the n-type and p-type silicon we mentioned earlier we need to be able to control the charge carrier concentrations in our silicon crystal this is done by a process called doping which is performed nowadays mainly through a process known as ion implantation. In this process dopant atoms (Group III -Group VI)

elements are vaporized, accelerated and directed at our Silicon substrate. Dopant depths can be controlled by adjusting the acceleration energy (ranging from 1 keV to 1 MeV) with depths from 100 Å to 10 μm and dopant dosing amounts can be controlled via the ion current with doses ranging from 10^{12} ions/cm^2 to 10^{18} ions/cm^2.

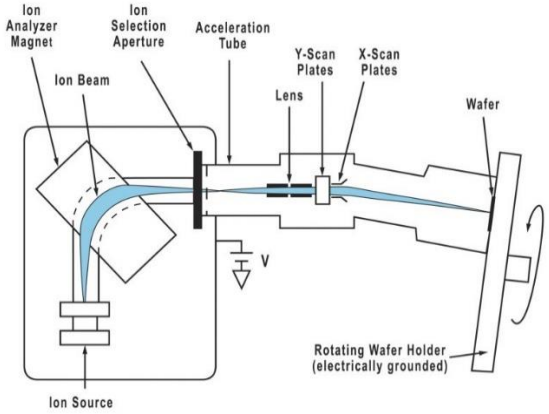


Fig. 16. Ion Implantation Device

After this the crystal ingot is ground down and sliced into its wafer substrate size.

3.1.3. Chemical Vapour Deposition

To create our SiO_2 layer for our MOSFET and for layering the substrate with dielectrics, insulators and conductors to be patterned by lithographic processes we require the use of chemical vapour deposition. CVD reacts a Silicon-containing gas (e.g. SiH_4) with an oxygen precursor leading to the deposition of SiO_2 in this case on the substrate. This is usually performed at a low pressure (~100 mTorr ≈ 13.3 Pa).

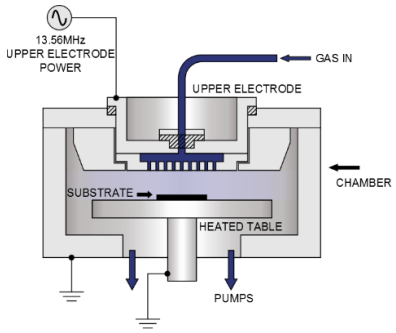


Fig. 17. Chemical Vapour Deposition Reactor

3.2. Pattern Transfer

To create the transistors "features" on the substrate we use a process called lithography which takes the circuit design and prints it onto the Silicon wafer. It is here that again the small feature sizes pursued by Moore's Law have begun to present problems for chip manufacturers.

3.2.1. Lithography

The circuit design is etched into a glass mask, this is the interconnected transistors we wish to transfer onto our Silicon substrate. Primarily UV light is used to shine through the mask and image the mask patterns onto the substrate.

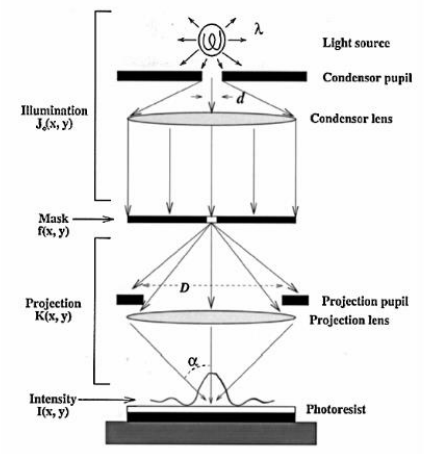


Fig. 18. Photolithography Process

The UV light reacts with a UV-light sensitive photo emulsion known as "photoresist" which is layered on with a thickness of about (~0.5 μm), the exposed regions of photoresist become acidic and are etched away with a basic solution such as NaOH. Exposure of wafers is performed for each die using a step and scan technique that moves through each processor core one-by-one. Multiple masks are used to build up the many intricate patterns of circuits.

3.2.2. The Limits of Lithography

Much like how quantum mechanics posed a problem for device miniaturisation so too does the photolithography process. Pattern dimensions have gotten to the scale

of the wavelength of light which causes serious problems for the resolution of photolithography systems and the accuracy of fabricated integrated circuit features. The simple geometrical laws of light do not apply, and its wave nature must be considered i.e. diffraction. The diffraction-limited feature size is given by **Eq. 4.**

$$l_{min} = 0.8\frac{\lambda}{NA}$$

Eq. 4. Diffraction-Limited Feature Size

where:

$$\lambda = Wavelength\ of\ Photolithographic\ Light\ Source$$

$$NA = Numerical\ Aperture\ Size\ of\ Lenses\ Used\ in\ Photolithography\ System$$

From this expression we can see that for smaller dimensioned transistors we need to use larger lenses or decrease the wavelength of the light we use.

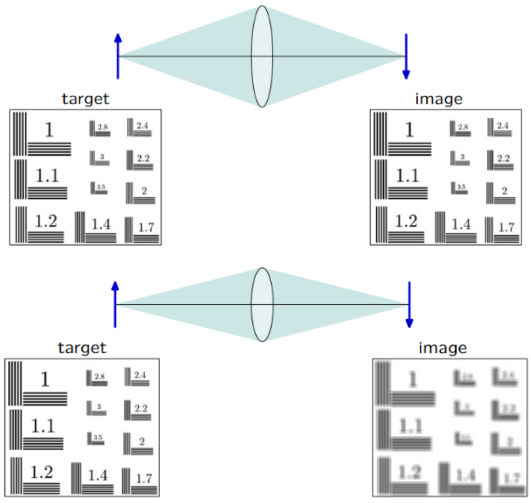


Fig. 19. Lens Diameter and Image Quality

Use of extremely clever exposure techniques which employ Fourier optics have so far been the main improvements in photolithographic systems, the future will require the use of light sources with shorter wavelengths. Electron beam lithography gives the highest feature resolutions but is a serial process as opposed to the parallel (one scan per chip die) process of conventional photolithography and therefore production throughput decreases dramatically for this method requiring

the electron beam to scan across the mask. One technique that allows us to use smaller feature sizes and has a production speed matching conventional lithography is extreme ultraviolet lithography.

3.2.3. Extreme Ultraviolet Lithography

Extreme ultraviolet lithography reduces the wavelength of the conventional lithographic process from 193-248 nm to 13.5 nm [Lit. 8.]. The EUVL system is far more demanding than conventional processes, requiring a vacuum environment and reflective rather than refractive optics, but has overcome most of its major technical hurdles and is mainly restricted by cost and reliability issues. The number one challenge remaining for cost effective implementation EUVL high volume manufacturing is the EUV source power. In a comparison of EUVL versus conventional lithographic source power in **[Lit. 8.]** it is found that to implement 10 EUVL scanners in place of 10 conventional scanners would require an additional 700 kW of power for a microchip fabrication facility. The high power is mainly due to the efficiency of the laser used to hit a droplet of tin to generate plasma which radiates the EUV light. Crucially the laser power requirements will need to be reduced (some researchers are experimenting with CO_2 lasers [Lit. 8.]).

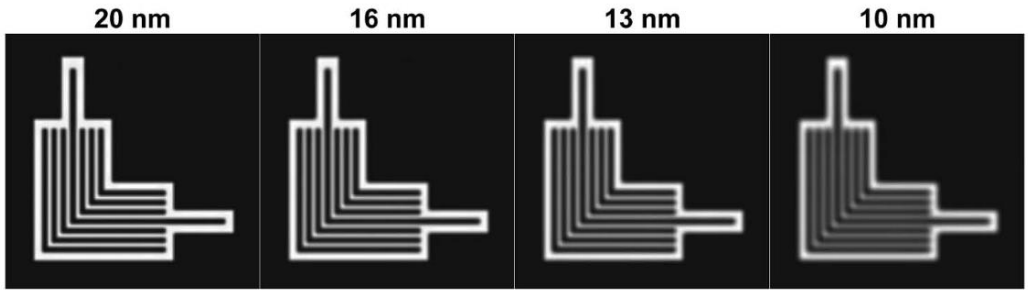


Fig. 20. 0.5-NA EUV Printing Under Disk Illumination with a Partial Coherence of 0.7

ASML in the Netherlands is leading the way in commercialisation of this technology shipping 10 of their TwinScan EUV systems in Q3 of 2020 [Lit. 9.].

4. Failure of Electronic Materials

Reliability of electronics has always been a pressing issue for safety critical applications and no one is more in need of that reliability than the military, this can be seen in the US Department of Defence's attempt to quantify the failure parameters for various electronic components in their Military Handbook 217 (MIL-HDBK-217) [Lit. 10.]. While we may not be examining military applications quantification of the reliability of solid state electronic devices matters to us if we are to design usable computer chips and so we shall look at the mechanisms for electronic device failure and methods for failure analysis in the following section.

4.1. Mechanisms for Failure

Electronic components will continue to function reliably if their response parameters which are resistance, voltage, current gain and capacitance remain within a certain tolerance of their chosen design values. These parameters each depend on environmental and material parameters which are temperature, humidity and semiconductor doping levels. "Irrespective of the specific mechanism, failure virtually always begins through a time-dependent movement of atoms, ions or electronic charge from benign sites in the component to harmful sites" [Lit. 11.]. What we would like to understand is what is the specific mechanism that causes the movement of matter or charge in the component and from there determine the magnitude of concentration at which the device fails.

4.1.1. Mass Transport-Induced Failure

One of the main culprits of mass transport-induced failure is electromigration, a phenomenon not unlike electrolysis, which occurs in the metallized components of chips i.e. interconnects, transmission lines and vias which carry electrical signals. While not exactly well understood physically it is believed that when current is flowing through a conductor, electrons moving towards the anode can strike ion cores imparting some amount of momentum to them causing them to be shunted into neighbouring vacant atomic sites.

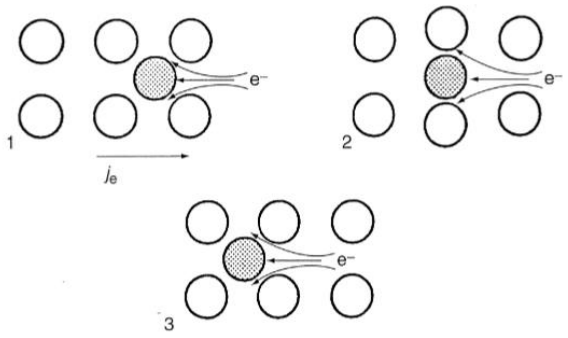


Fig. 21. Atomic model for electromigration

Electromigration primarily occurs in the metallized contacts between the chip and the motherboard. Ondrusek [Lit. 12.] et al. have studied Al-Si and $TaSi_2$-Si contacts and has found that Al-Si contacts fail with an activation energy of 0.9 eV whereas $TaSi_2$-Si contacts fail with an activation energy ranging from 1.1 to 1.4 eV, so contact longevity can be increased through use of $TaSi_2$ as a connector material.

4.1.2. Electronic Charge-Induced Failure

Failure via transport of electrons effects insulators and capacitors and one of the primary mechanisms for this type of failure is dielectric breakdown.

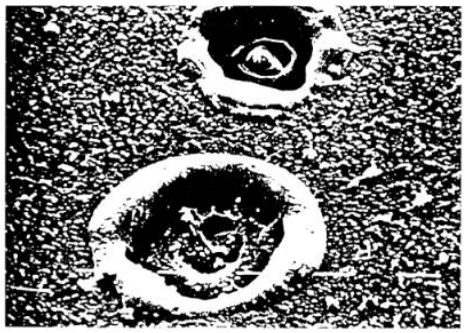


Fig. 22. Scanning Electron Micrograph of Dielectric Breakdown in SiO_2 Layer (Crater Diameter ~3 μm)

This failure mechanism is a likened to mechanical fracture. A voltage (stress) applied to a component produces a flow of charge (elongation). Electrical energy is stored according to the capacitance formula $\frac{1}{2}CV^2$ ($\frac{1}{2}Ee^2$). Above a certain electric field strength (beyond elastic range) charge is injected into the dielectric and electrical energy is converted into heat (mechanical energy converted to heat via

dislocation gliding). When the injected charges (strains) go beyond a critical value the material abruptly loses its stored energy.

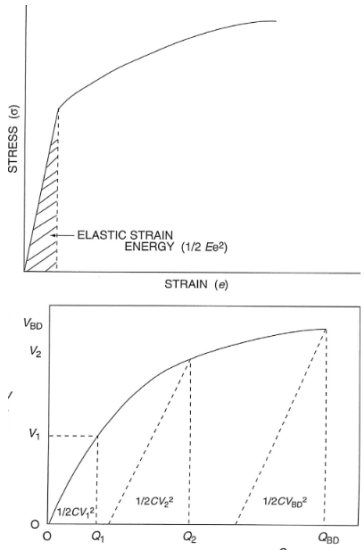


Fig. 23. Analogy Between Dielectric Breakdown and Mechanical Fracture

4.2. Failure Analysis

Having seen some of the ways in which device failure can be initiated we'll now briefly look at failure analysis methods for electronic devices.

4.2.1. Non-destructive Analysis

Ideally when analysing the failure of any material is preferred to keep the specimen intact and one important method in electronic device failure investigation is the use of scanning acoustic microscopy. Similar in principle to ultrasound, it relies on generating sound waves with a piezoelectric transducer and scanning them across the chip to be analysed. Reflected waves are processed and images are built from variations in acoustic impedances.

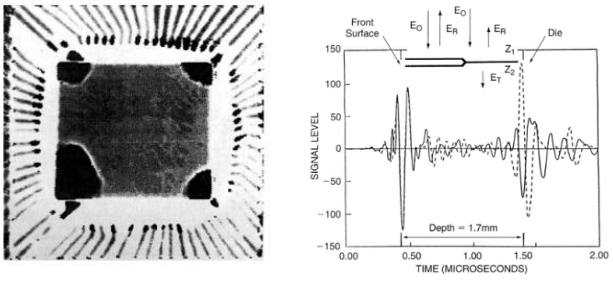


Fig. 24. SAM Image of Chip Die and Acoustic Echo Signals from SAM Analysis

From the graph and acoustic echo level output as shown in **Fig. 24.** bonded and un-bonded (failed) contacts. If the cause of failure has not been determined via non-destructive methods chip de-capping will be required which involves removing the protective packaging of the Silicon die.

4.2.2. Electrical Stress Tests

The previous method falls short in that the failure is not viewed under use conditions to do this we require the device to be powered or heated to a certain level that would be normal for operating conditions and analyse it. To observe heating a charge transport effects the use of light emission microscopy is required which via optically stimulation of the die causes luminescence at defect sites which can be picked up by the microscope.

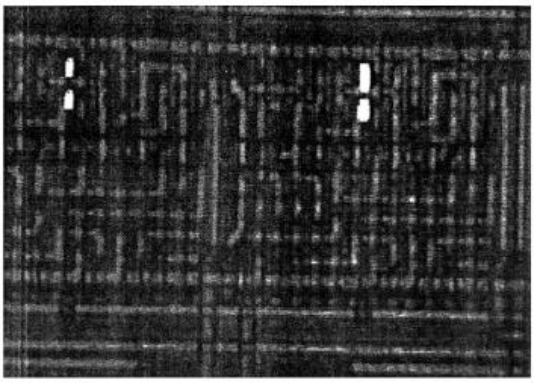


Fig. 25. Light Emission Image of Chip Die (n-channel Transistors Illuminated)

4.3. How Device Scaling Affects Failure

Device miniaturisation pushes materials to their limits and decreases longevity. Primarily device lifetimes are decreased by a factor of K^8 **[Lit. 11.]** where K is the device scaling (reduction) factor.

As a side note if we want to keep pushing the speed of computer chips, we run into a fundamental material limit, known as the transit time of an electron t_d which determines the switching time of a gate. For Silicon this limit stands at about 5×10^{-15} seconds [Lit. 11.] beyond which transition times cannot be improved.

5. End of Life and Sustainability of Electronic Materials

So, after a chip has failed what options do we have in terms of being able to recover materials? This is an extremely pressing issue as e-waste is the fastest growing waste stream in the world estimated to be about 8% of all municipal waste worldwide [Lit. 13.] and the electronics industry is incredibly resource intensive.

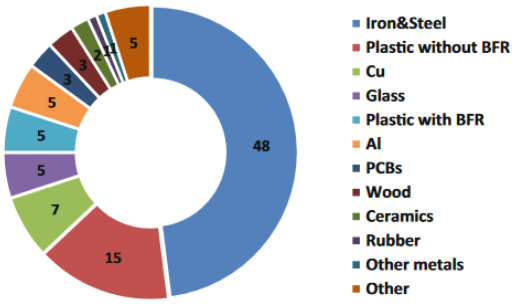


Fig. 26. Percent Main Materials Found in Electrical and Electronic Equipment

The largest issue with the resource use of the semiconductor industry is the fact that it relies heavily on the use of metals with dwindling supplies in its products and processes as seen in **Fig. 27.** around 60 valuable elements from the periodic table are used in the electronics manufacturing process [Lit. 13.]. Precious metals recovery is of utmost importance for any recycling process that is developed, especially considering that a quarter of all Copper produced globally on an annual basis is earmarked for use in electronic device manufacturing And 320 tonnes of Gold and 7,500 tonnes of Silver are used along with it [Lit. 13.].

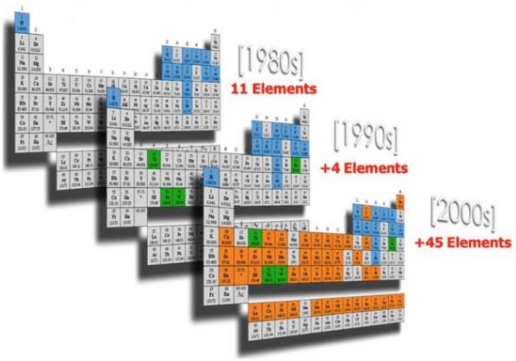


Fig. 27. Increase of Precious Metals Used in Electronic Circuitry Over the Years

From a social standpoint we need able to process electronic waste in our country cheaply and safely where the electronics are being purchased by consumers rather than being shipped for

processing to foreign countries where worker safety laws go by the wayside. In **Fig. 28.** Below we see some of these poor women, children and prisoners from areas of China and India working at crude e-waste recycling facilities without any personal protective equipment. Two of the most notorious areas for unregulated e-waste processing are the Guangdong Province in South China and the Zhejiang Province in East China [Lit. 13.].

Fig. 28. Illegal E-Waste Recycling Facilities in China and India

5.1. Component and Printed Circuit Board Recycling Chain

Let's look at the current methods for recycling of components and printed circuit boards (PCB's).

5.1.1. Pre-processing

Pre processing starts with the dismantling and de-soldering of components. On industrial scales solder is dissolved using chemical reagents such as molten salts (such as LiCl-KCl). This has raised environmental concerns due to the high toxicity of run-off, however manual de-soldering as an alternative has a major cost implication, one possible solution is the use of wet chemical selective de-soldering to reduce the environmental impact [Lit. 13.]. After that a size reduction process is applied via means of a shredder in most common applications with particle sizes of about (< 50mm). These particles are sorted via a combination of wet, dry and gravity separation methods and are ready for the materials recovery process.

Fig. 29. Zig-Zag Separator (Dry-Gravity Process) (Left)
Cyclone Separator (Wet-Gravity Process) (Right)

5.1.2. Materials Recovery

If we wish to retrieve the precious metals that were used to create these devices we must use a hydrometallurgical process to "leach" the metal out of the rest of the crushed particle we now have, again like the de-soldering process the use of leaching solutions creates a considerable amount of waste and so care must be taken in choosing methods of material recovery.

ATMI Inc. have developed a very efficient and environmentally benign automatic de-soldering and precious metal recovery system. The solder is soaked in an acidic solution for 20 minutes at around 30 to 40 °C and is collected as a salt and resold. The recovered integrated circuits if still functioning can be re-used or if not can be ground down with Silver recovery efficiency above 99% and Copper recovery above 95% [Lit. 13.].

Fig. 30. ATMI Precious Metal Recovery System

5.2. Umicore's Integrated Smelters-Refineries, Hoboken, Antwerp

To see the cutting edge of precious metals recovery in action we'll briefly look at the operations of a Belgian metal refinery in Antwerp, Umicore.

Fig. 31. Umicore Facility Antwerp

Umicore is one of the most advanced precious metal recycling facilities in the world processing some 250,000 tonnes of e-waste per year, a Gold recovery rate of 95% for the plant has been reported [Lit. 13.]. The workhorse of the plant, the smelter, operates off a Top Submerged Lance combustion technique [Lit. 14.], the simple operation allows for great flexibility in the recovery process. Most importantly environmental impact is minimal, when recovering 75,000 tonnes of metal from 300,000 tonnes of recyclables, 3.73 tonnes of CO_2 per tonne of recovered metal is generated compared to an average of 17.1 tonnes of CO_2 per tonne of recovered metal via conventional means [Lit. 13].

6. Conclusions and The Future of Computing Materials

To close out, how should computer chip materials change to **a)** increase reliability and reduce environmental impact and **b)** combat the plateauing of Moore's Law.

Restricted to our current chosen materials and current reliability of electronic devices how can we improve on our e-waste recycling technologies. While Umicore and the ATMI programs may seem to be combatting e-waste these facilities stand alone in terms of technology. If higher yield rates for metal recovery could be achieved process costs would be offset by the relative value of reselling these metals to the electronics market. While Umicore' process is rather environmentally friendly the use of pyrometallurgy is still quite harmful and so a move to

hydrometallurgical methods such as the ATMI method would be a more environmentally sound move.

If we increase device reliability of course recycling benefits as we have less need for recycling of e-waste each year. In general, the most cost-effective road lies with manufacturing in terms of reliability improvements as shown in **Fig. 32.** adapted from an article by D.L. Crook in the IEEE Reliability Physics Symposium Journal [Lit. 15.].

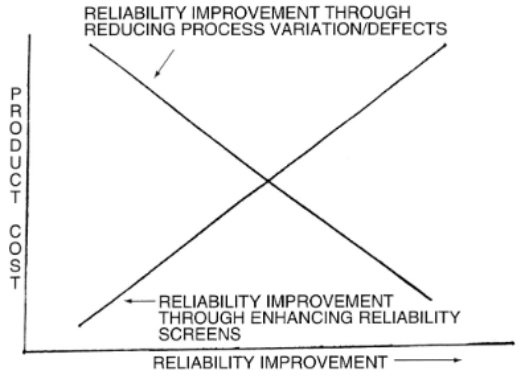


Fig. 32. Economic Implications of Building-In and Testing-In Philosophies for Improving Reliability

While we could use electrical stress tests for quality control this would greatly increase product cost and fabrication times. No to discount these failure analysis methods entirely of course it is important to integrate what has been learnt from failure tests to inform the manufacturing process.

Finally, what's on the horizon in terms of the material technologies available to overcome the fundamental limitations of Silicon and keep increasing computational power, certainly extreme ultraviolet lithography is pushing the limits of manufacturing, here I've outlined two possible radical solutions that are in development:

6.1. A Single-Atom Transistor

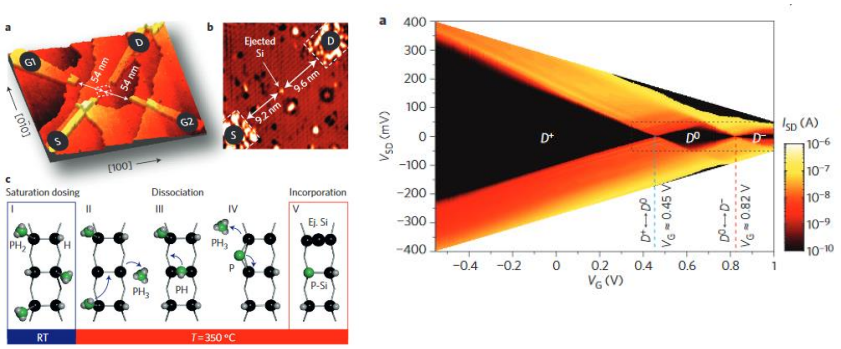


Fig. 33. Single-Atom Transistor Created Using Phosphor Atom Embedded in Silicon (Left) Experimental Results for Gate Voltage against Source-Drain Voltage and Current (Right)

A paper by Michelle Simmons' team at UNSW [Lit. 16.] put forward some ground-breaking research that is central to the creation of quantum computers and other computationally devices based on electron spin. Ultimately the success of quantum technology lies on the precise placement of dopants within a Silicon matrix and within this paper we have seen just that. This technology has the potential for great space savings with a source to drain distance of roughly 19 nm in the technology's infancy, this size has scope for reduction. Since this device is quantum based, operating off higher throughput qubit information processing allowing for the storing of 4 different levels of information in one "bit". However current methods of Phosphor atom implantation are not suitable for manufacturing requiring the use of a scanning tunnelling microscope.

6.2. Carbon-Nanotube Field Effect Transistor

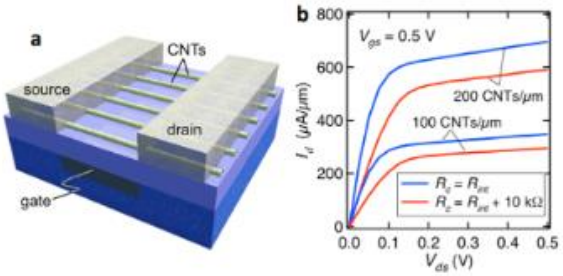


Fig. 34. Carbon Nanotube Field-Effect Transistor and Device Voltage Current Characteristic

Another novel material technology being developed is carbon nanotube-based transistors. Being an inherently 1D channel, quantum effects are confined within the nanotube combatting tunnelling effects as devices are miniaturised. However success of this technology requires the implementation of a device that has several carbon nanotube channel (i.e. several carbon nanotubes) **[Lit. 17]**.

As we can see the challenges facing the continued innovation of the semiconductor industry need to be tackled on many fronts and it will take a combination of efforts in the areas outlined above to see continued progress.

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Figure 2. NAND Logic Gate**,** Maxim Integrated: https://www.maximintegrated.com/en/glossary/definitions.mvp/term/NAND%20Gate/gpk/1203

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Figure 5. Common Semiconductor Materials Table:
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Figure 7. Point Defects in a Silicon Lattice:
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Figure 10. Junction Field-Effect Transistor:
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Figure 11. Transistor Count on Integrated Circuit versus Year "Moore's Law":
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Figure 14. Czochralski Crystal Furnace and Puller Device, ECM Lab Solutions:
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Figure 15. Four-Point Probe Resistivity Measurement, PV Education**:**
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Figure 18. Photolithography Process:
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Figure 19. Lens Diameter and Image Quality:
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Figure 24. SAM Image of Chip Die and Acoustic Echo Signals from SAM Analysis:
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Figure 26. Percent Main Materials Found in Electrical and Electronic Equipment:
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Figure 30. ATMI Precious Metal Recovery System:
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Figure 31. Umicore Facility Antwerp:
https://commons.wikimedia.org/wiki/File:Umicore_Hoboken_4.JPG

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Figure 33. Single-Atom Transistor Created Using Phosphor Atom Embedded in Silicon and Experimental Results for Gate Voltage against Source-Drain Voltage and Current:
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